VISHWKARMA GOVERNMENT ENGINEERING COLLEGE, CHANDKHEDA

Report on

One week FDP on "Research Opportunities in VLSI and Signal Processing"

Name of Department/Organizer	:	Electronics & Communication Department and IEI Student Chapter
Date & Time	:	11/02/2019 to 16/02/2019
Venue	:	Ahmedabad
No of Participants	:	**40**

EC Department of Vishwakarma Government Engineering College Chandkheda has organized ISTE-GTU Sponsored Faculty Development Programme (FDP) on "Research Opportunities in VLSI and Signal Processing" from 11th February to 16th February, 2019. Dr R.A.Thakker was coordinator and Dr M.S.Shah was co-coordinator of this FDP.More than 40 participants including PG students have participated in this training program.

The objective of this FDP is to aware faculty members with recent developments and research opportunities in VLSI and Signal Processing. Experts from IIT – Gandhi agar, DAIICT, Nirma University and VGEC - Chandkheda have shared their knowledge and research work with participants. Hand-on-sessions with the support of experts from Industry were also arranged to provide exposure of latest computer simulation tools to the participants. It will help participants to decide their topic of research work in further study.

First day:

Inauguration Ceremony:

In the auspicious presence of Dr. Navin Sheth (Vice-Chancellor – GTU), the inaugural ceremony of FDP was held in the campus of VGEC – Chandkheda. It was also attended by Shri. Damodara M S, Business Manager, Entuple Technologies, Prof. S. P. Sapre, I/C Principal, VGEC Chandkheda, Dr. R. A. Thakkar, Coordinator of this FDP and HoD - EC and Dr. N. M. Patel, Associate Professor, Chemical Department and Dr. A. R. Patel, Associate Professor - Mathematics.

Dr. R. A. Thakkar, Coordinator of this FDP had given the opening remarks, briefed about the course contents, objective of the training program and shared his views on Research Opportunities in VLSI and Signal Processing.

Dr. Navin Sheth stated that "Teachers should be one step ahead of Student in Technology updates and Knowledge". He emphasized on the skills of delivery of knowledge along with gathering of information. He also stated that small appreciation of students will make large change in student learning which makes them good human being and great technocrat of future.

Shri, Damodara M. S. who has been working in the field of Chip Designing since 2001 said that "The globally one third of investment is happening in Electronics System Design and Manufacturing". In near future, Electronics Market in India will rise to 400Bn $ which will generate 27.5 million job opportunities in the field of Electronics in India. Every year in India, 1.5 million of engineering graduate receive their degree. Hence, it is a huge opportunities for students and researchers in this field.

Prof. S. P. Sapre mentioned that faculties should be trained on continuous basis to improve the quality of teaching. VGEC – Chandkheda not only permits and motivates faculty to attend FDPs but also encourages for organization of such FDPs.

First session after inauguration was taken by Dr R.A.Thakker, Coordinator of this FDP on "FinFET based circuit design". He has discussed advantages of using FinFET over MOSFET and various circuits based on FinFET from research papers.

Second and Third session of first day was conducted by experts from entuple technologies Mr. Swapnil Moon and Mr. Sumit Patil.They have given overview of Cadence EDA Tool and MOS fundamentals and CMOS circuit Design. In the hands on session participants have done design simulation, layout, and parasitic extraction, DRC Vs LVS check, and post layout simulation of CMOS inverter.

Second day:

First and Second session was Lab sessions for EDA Tools conducted by Mr. Swapnil Moon and Mr. Sumit Patil.In this Sessions Device characterization for Analog model parameters has been done.With the review of generic amplifier performance parameters and interpretation of design parameters ,example of CS Amplifier is discussed and design of CS Amplifier is simulated by participants in the lab session for various AC and DC parameters and sessions were highly useful for understanding concepts of Analog circuit Design using MOSFETs.

Third session was taken by Dr Nihar Mahapatra, Associate Professor from IIT Gandhinagar.His topic was"CMOS device technologies for circuit design-Past, Present and Future". He discussed evolution of CMOS technology from 4 bit microprocessor to advance microprocessors. He also showed 12 inch silicon wafer to get physical feel of fabrication technology.

Third Day:

First session of third day was taken by Dr Joycee M Mekie; Associate Professor from IIT Gandhinagar.Her topic was "Approximate memories for Multimedia Applications". She mentioned that Image processing and other multimedia applications require large embedded storage so requirement of power and area efficient memory design is need of the hour and approximate memory will be one the solution for it.

Second and third session was lab sessions for ASIC Design flow and synthesis of HDL design using RTL compiler. In sessions participants have written HDL Codes and with the help of RTL Compiler tool done the simulation and synthesis of HDL codes and analysis of the reports generated by tool. The three day Lab session from experts of entuple technologies was highly fruitful and beneficiary to the entire participant and encouraged and ignited them to do the research in the field of VLSI domain.

Fourth Day:

First session of Forth day was taken by Dr Nitin George; Associate Professor from IIT Gandhinagar.His topic was “Adaptive Signal Processing”. He talked about fundamentals of adaptive signals and with example of two speaker system in mobile phone he explained application and advantages of adaptive signal processing in real world.

Second session was taken by Dr M V Joshi; Professor at DAIICT, Gandhinagr.His topic was “Machine Learning”. He gave the complete overview of machine learning. He mentioned how machine learning is playing in key role in day to day life with some applications.

Third session was conducted by Dr.Rutu Parekh, Assistant Professor from DAIICT, and Gandhinagar on “Nano electronics”. She talked about the current and future activity and research going in the field of nano electronics. She has expressed the need of acceleration in discovery and use of novel nanoscale fabrication processes and innovative concepts to produce revolutionary materials, devices, systems, and architectures to advance the field of nanoelectronics is requirement of the day.

Fifth Day:

First session was taken by Dr.Usha Mehta, Professor at Nirma University, Ahmedabad on “Overview of testing & Verification of VLSI Design”. She has explained complete testing flow and discussed the bottle neck in the field of testing. With examples of various bugs occurred in various IC’s she said that bugs free design does not give extra revenue but bugs in design are very costly.

Second session was conducted by Dr.N P Gajjar, Professor at Nirma University, and Ahmedabad on “VLSI signal processing system”. He has discussed various signal processors used in VLSI domain. He pressed the need of use of Reconfigurable processor architecture in Design with the other innovative steps in order to do faster processing of data.

Third session was conducted by Dr.A B Nandurbarkar, Associate Professor at L D College of Engineering, and Ahmedabad on “Speech Signal Processing”. He nicely explained analysis and synthesis of speech signals. He has also shared various PG/PhD level research topics in the field of Video, image and speech processing with the participants.

Sixth Day

First session was conducted by Dr C H Vithalani, Professor at GEC, Rajkot on “Signal Analysis using Wavelet transfrom”.He gave comparison of various available transforms and shown usefulness of Wavelet transform in Signal Analysis domain with the help the mathematical equations. He also narrated various methods for signal analysis.

Second session was conducted by Mr Usmesh Patel, CEO, and Arastu system on “DSP based industry applications.”.He explained the current status and market growth of semiconductor industry and role of industry in EDA design. He discussed various DSP based industry applications and role of it making the industry process smarter and fast and cost effective.

Valedictory Function:

The FDP was concluded with the valedictory function in which the participants were given their participation Certificates in presence of Dr. K.M. Bhavsar, Chairman, ISTE Gujarat Section, Dr.S.D Panchal(I/C Registrar GTU),Dr R K Gajjar(Principal VGEC,Chandkheda) ,Dr R.A.Thakker (Coordinator of FDP) and HOD's of all department and faculty members of college.

Feedback of participants:

-'Excellent hands on session in Labs and all other sessions were also quite useful'

Dr.A.B.Nandurbarkar, LDCE, Ahmedabad

-'Overall management, Hospitability of FDP and delivery of lecture by experts and lab sessions are impressive.'

Tejas Shah, SSEC, Bhavnagar


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